IN THE SPECIFICATION

The title paragraph beginning at page 1, line 1 is amended as follows:

~~DRAM~~ SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

The paragraph beginning at page 1, line 4 is amended as follows:

Cross Reference To Related Applications

This application is related to the following co-pending, commonly assigned U.S. patent applications: "DRAM Cells with Repressed Memory Metal Oxide Tunnel Insulators," attorney docket no. 1303.019US1, ~~serial number~~ serial number 09/945,395, "Programmable Array Logic or Memory Devices with Asymmetrical Tunnel Barriers," attorney docket no. 1303.020US1, ~~serial number~~ serial number 09/943,134, "Dynamic Electrically Alterable Programmable Memory with Insulating Metal Oxide Interpoly Insulators," attorney docket no. 1303.024US1, ~~serial number~~ serial number 09/945,498, and "Field Programmable Logic Arrays with Metal Oxide and/or Low Tunnel Barrier Interpoly Insulators," attorney docket no. 1303.027US1, ~~serial number~~ serial number 09/945,512, "Flash Memory with Low Tunnel Barrier Interpoly Insulators," attorney docket no. 1303.014US1, ~~serial number~~ serial number 09/945,507, "Programmable Memory Address and Decode Devices with Low Tunnel Barrier Interpoly Insulators," attorney docket no. ~~(Micron 01-0485)~~1303.029US1, ~~serial number~~ serial number 09/945,500, ["SRAM Cells with Repressed Floating Gate Memory, Low Tunnel Barrier Interpoly Insulators Insulators," attorney docket no. 1303.019US1, serial number_____ ,] which are filed on even date herewith and each of which disclosure is herein incorporated by reference.

The paragraph beginning at page 10, line 25 is amended as follows:

According to the teachings of the present invention, the non-volatile memory component includes a low tunnel barrier intergate, or interpoly, insulator between the control gate and the floating gate. An example is shown in Figure 4. According to the teachings of the present invention. According to the teachings of the present invention, the low tunnel barrier intergate insulator can include aluminum oxide, transition metal oxides, and perovskite oxide tunnel

barriers, and others of the like, between the floating gate and control gate. An example for these metal oxide intergate insulators has been described in detail in the copending, co-filed application entitled, "Flash Memory with Low Tunnel Barrier Interpoly Insulators," attorney docket no. 1303.014US1, serial no. 09/945,507 ~~serial number _____~~. The use of metal oxide films for this purpose offer a number of advantages including: